Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) An EEPROM device having a lower programming voltage, said EEPROM device comprising:

a programming capacitor configured within a polysilicon layer;

a tunneling region configured within said polysilicon layer; and

a drawing layer comprising at least one serrated element configured underneath said tunneling region, said at least one serrated element configured to provide a restriction of oxygen used to grow gate oxide for determining programming voltage of said EEPROM device.

2. (Original) The EEPROM device according to claim 1, wherein said at least one serrated element comprises a wider region reducing to a narrower region, said narrower region configured for restricting oxygen when drawing corners under polysilicon during a semiconductor manufacturing process resulting in a reduced growth of said gate oxide.

3. (Original) The EEPROM device according to claim 1, wherein said at least one serrated element comprises at least one acute angle structure configured within an active mask drawing layer, said at least one acute angle structure having an acute angle region configured for restriction of growth of said gate oxide.

4. (Original) The EEPROM device according to claim 3, wherein said acute angle region comprises an acute angle between greater than zero degrees and less than 180 degrees.

5. (Original) The EEPROM device according to claim 4, wherein said acute angle region comprises an acute angle between approximately 75 and 105 degrees.

6. (Original) The EEPROM device according to claim 1, wherein said at least one serrated element comprises at least one of a rectangular, pentagonal, hexagonal, and semi-circular region having an opened region and a more narrowed region configured for restriction of growth of said gate oxide.

7. (Original) The EEPROM device according to claim 1, wherein said EEPROM device comprises at least two serrated elements configured in a staggered arrangement to allow for misalignment between an active layer and a polysilicon layer.

8. (Original) The EEPROM device according to claim 1, wherein said EEPROM device comprises a double-bit configuration comprising a second programming capacitor and a second tunneling region, and at least one serrated element configured underneath said second tunneling region and configured to restrict oxygen used to grow gate oxide for determining programming voltage of said EEPROM device.

9. (Original) An analog integrated circuit comprising:

an analog device configured for providing an output signal; and

an EEPROM device configured for on-chip calibration of said analog device, said EEPROM device comprising:

a programming capacitor configured within a polysilicon layer for providing a WRITE signal input;

a tunneling region configured within said polysilicon layer for providing an ERASE signal input; and

a drawing layer comprising at least one serrated element configured underneath said tunneling region to restrict growth of gate oxide, thus lowering a required programming voltage of said EEPROM device.

10. (Original) The analog integrated circuit according to claim 9, wherein said at least one serrated element comprises an wider region and a narrower region, said narrower region configured for restricting oxygen when drawing corners under a polysilicon layer during a semiconductor manufacturing process resulting in a reduced growth of said gate oxide.

11. (Original) The analog integrated circuit according to claim 9, wherein said at least one serrated element comprises at least one acute angle structure configured within an active mask drawing layer, said at least one acute angle structure having an acute angle region configured for restriction of growth of said gate oxide.

12. (Original) The analog integrated circuit according to claim 11, wherein said acute angle region comprises an acute angle between approximately 75 and 105 degrees.

13. (Original) The analog integrated circuit according to claim 9, wherein said at least one serrated element comprises at least one of a rectangular, pentagonal, hexagonal, and semi-circular region having an opened region and a more narrowed region configured for restriction of growth of said gate oxide.

14. (Original) The analog integrated circuit according to claim 9, wherein said EEPROM device comprises at least two serrated elements configured in a staggered arrangement to allow for misalignment between an active layer and a polysilicon layer.

15. (Original) The EEPROM device according to claim 9, wherein said EEPROM device comprises a double-bit configuration comprising a second programming capacitor and a second tunneling region, and at least one serrated element configured underneath said second tunneling region and configured to restrict oxygen used to grow gate oxide for determining programming voltage of said EEPROM device.

16. (Original) A method for providing a lower programming voltage in an EEPROM device, said method comprising the steps of:

modifying a mask drawing layer with at least one serrated element configured underneath a tunneling region of the EEPROM device; and

restricting oxygen proximate said at least one serrated element when forming a gate oxide region underneath said tunneling region resulting in a thinner gate oxide region being formed.

17. (Original) The method according to claim 16, wherein said step of modifying said mask drawing layer comprises providing a thin oxide region configured to restrict oxygen used for growing gate oxide.

18. (Original) The method according to claim 16, wherein said step of modifying said mask drawing layer comprises modifying an active mask drawing layer with at least one acute angle structure configured to provide said thinner gate oxide region.

19. (Original) The method according to claim 16, wherein said step of modifying said mask drawing layer comprises modifying an active mask drawing layer with a structure having an wider portion and a narrower portion configured to provide said thinner gate oxide region.

20. (Original) The method according to claim 16, wherein said step of modifying said mask drawing layer comprises staggering at least two serrated elements to allow for misalignment of an active layer and a polysilicon layer.

21. (Original) An EEPROM device requiring a lower programming voltage, said EEPROM device comprising:

a programming capacitor;

a tunneling region configured in a layer proximate to said programming capacitor; and

at least one serrated element configured underneath said tunneling region, said at least one serrated element configured to restrict growth of gate oxide to reduce requirements for programming voltage of said EEPROM device.

22. (Original) The EEPROM device according to claim 21, wherein said at least one serrated element is configured to provide a restriction of oxygen used to grow said gate oxide.

23. (Original) The EEPROM device according to claim 22, wherein said at least one serrated element comprises a thinned region configured to provide said restriction in oxygen.

24. (Original) The EEPROM device according to claim 21, wherein said at least one serrated element comprises an opened region reducing to a narrowed region, said narrowed region configured for restricting oxygen when drawing corners under polysilicon during a semiconductor manufacturing process resulting in a reduced growth of said gate oxide.

25. (Original) The EEPROM device according to claim 21, wherein said at least one serrated element comprises at least one acute angle structure configured within an active mask drawing layer.

26. (Original) The EEPROM device according to claim 25, wherein said acute angle region comprises an acute angle between approximately 75 and 105 degrees.

27. (Original) The EEPROM device according to claim 21, wherein said EEPROM device comprises at least two serrated elements configured in a staggered arrangement to allow for misalignment between an active layer and a polysilicon layer.

28. (Original) The EEPROM device according to claim 21, wherein said EEPROM device comprises a distributed-gate configuration.

29. (Original) An analog integrated circuit comprising:

an analog device configured for providing an output signal; and

an EEPROM device configured calibration of said analog device, said EEPROM device comprising:

a programming capacitor;

a tunneling region configured in a layer proximate to said programming capacitor; and

at least one serrated element configured underneath said tunneling region to restrict growth of gate oxide, thus lowering a required programming voltage of said EEPROM device.

30. (Original) The analog integrated circuit according to claim 29, wherein said at least one serrated element comprises an wider region and a narrower region, said narrower region configured for restricting oxygen when drawing corners under a polysilicon layer during a semiconductor manufacturing process resulting in a reduced growth of said gate oxide.

31. (Original) The analog integrated circuit according to claim 29, wherein said at least one serrated element is configured to enable said EEPROM device to utilize a programming voltage of less than approximately 8.8 volts.

32. (Original) The analog integrated circuit according to claim 29, wherein said at least one serrated element is configured to enable said EEPROM device to utilize a programming voltage generated by a charge pump using less than approximately 3 microamps.

33. (New) An EEPROM device comprising:

a tunneling region configured within a polysilicon layer; and

at least one serrated element configured underneath said tunneling region, to provide a restriction of oxygen.